

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLN. OF: TAKANO et al.  
SERIAL NO.: 10/648,995  
FILED: August 27, 2003  
FOR: Semiconductor Integrated Circuit Having Logic Circuit Comprising...  
DOCKET: NEC OSP-9770 DIV II

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

In connection with the above-entitled matter, Applicants hereby attach U.S. Patent Office form PTO-1449, including copies of the references listed therein. Where available, English language counterparts and/or abstracts are being provided for Examiner's convenience. These references were cited in the Japanese Office Action dated August 5, 2003 of the underlying Japanese patent application. Enclosed is a copy of the Japanese Office Action, together with an English translation of the relevant portions thereof. The claims in the present application are believed to be patentably distinguished over these references.

This Supplemental Information Disclosure statement is being made pursuant to the duty of disclosure imposed by law and formulated in 37 CFR 1.56(A). No representation is made that the information thus disclosed in fact constitutes prior art or that it is the closest prior art, inasmuch as 37 CFR 1.56(A) relies on a materiality concept which depends on subjectivity.

In compliance with the requirements of 37 C.F.R. § 1.98(a)(3), as a concise statement of relevance, as it is presently understood by the individual designated in 35 U.S.C. § 1.56(c) most

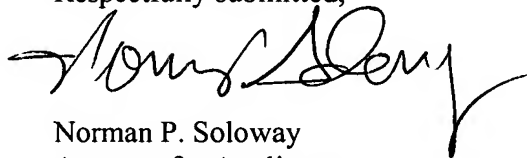
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knowledgeable about the content of the information, the undersigned attorney of record submits a translation of portions of an official action by a foreign examiner in which the references were cited. The relevance to the pending U.S. patent application is that the references were cited in a foreign patent application on the same subject matter. However, no independent analysis of the references, the accuracy of the statement of foreign examiner or the claims of the foreign application under the laws of the country or the United States relative to the subject matter claimed in the present application has been made; the present understanding of the contents thereof by the undersigned being based on the translation of the foreign examiner's comments submitted therewith.

The enclosed Supplemental Information Disclosure Statement is being submitted within three months of the Japanese Office Action, as certified in the attached Certification for Information Disclosure Statement. Therefore, we believe there are no fees involved with this Information Disclosure Statement. In the event there are additional fees payable, please charge them to our Deposit Account No. 08-1391.

Respectfully submitted,



Norman P. Soloway  
Attorney for Applicants  
Registration No. 24,315

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 9, 2003 at Tucson, Arizona.

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**STATEMENT UNDER 37 CFR 1.97(e) ACCOMPANYING  
INFORMATION DISCLOSURE STATEMENT**

Docket No.  
NEC OSP-9770 DIV II

In Re Application Of: TAKANO et al.

Serial No.  
10/648,995

Filing Date  
August 27, 2003

Examiner

Group Art Unit

Invention: Semiconductor Integrated Circuit Having Logic Circuit Comprising Transistors with Lower Threshold Voltage Values and Improved Pattern Layout

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

This is a statement under the provisions of 37 CFR 1.97(e) in the above-identified application.

Check applicable statement herebelow:

Statement Under 37 CFR 1.97(e)(1)

- ☒ Each item of information contained in the accompanying Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement.

Statement Under 37 CFR 1.97(e)(2)

- ☐ No item of information contained in the accompanying Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned person, after making reasonable inquiry, no item of information contained in the accompanying Information Disclosure Statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

  
Signature

Dated: October 9, 2003

Norman P. Soloway  
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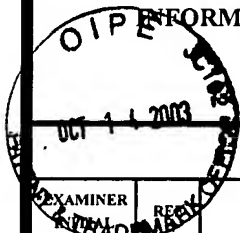
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Signature of Person Mailing Correspondence

Kathryn Grimes

Typed or Printed Name of Person Mailing Correspondence

CC:



## INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

NEC OSP-9770 DIV II

Application Number

10/648,995

Applicant(s)

TAKANO et al.

Filing Date

August 27, 2003

Group Art Unit

## U.S. PATENT DOCUMENTS

EXAMINER	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,078,195	6.20.00	CHEN	326	121	

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		09-200036	7.31.97	JAPAN (w/abstract)	H03K	19/08		✓
		02-082716	3.23.90	JAPAN (w/abstract)	H03K	19/0185		✓
		11-017522	1.22.99	JAPAN (w/abstract)	H03K	19/0944		✓
		WO 01/67609	9.13.01	PCT	H03K	19/00		

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)


EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and no considered. Include copy of this form with next communication to applicant.